

# **EFM<sup>®</sup>32**

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## **Errata, Chip rev B**

**EFM32G840F128/EFM32G840F64/EFM32G840F32**



This document describes known erratas for the EFM32G840.

# 1 Errata

## 1.1 Revision Identification

Please see the EFM32G840 datasheet for a description on how to extract the chip revision number.

## 1.2 Device revision B

**Table 1.1. Erratas**

ID	Title/Problem	Effect	Fix/Workaround	Resolved in rev C?
ADC4	<b>ADC 1 Msample/s</b> 1 Msample/s is not achieved for default ADC bias settings.	At default ADC bias settings the ADC conversion results are wrong when running the ADC_CLK at 13 MHz, which is required to reach the 1 Msample/s performance. Under typical conditions wrong conversions have been observed for ADC_CLK speeds of 8 MHz and higher.	Increase the ADC performance by programming increased ADC bias, for example by using value 0xF0F for register ADCn_BIASPROG.	Yes
ADC6	<b>ADC Reference Settling</b> The ADC internal references, i.e. 1V25, 2V5 and VDD have a settling time of about 500 us.	Measurements done using one of the internal references will not be correct before the reference has settled. This effect appears when switching between references and when the references have been off between samples.	When using the internal references, set WARMUP-MODE=3 in ADCn_CTRL and wait until the references have settled before taking the first sample.	Yes
ADC7	<b>ADC Accuracy</b> The ADC does not meet the specified accuracy of 11.7 effective bits.	The ADC accuracy may vary depending on the ADC configuration and may in some cases be down to 10 effective bits.	Using the hardware oversampling feature will increase the effective number of bits.	Yes
ADC8	<b>ADC Temperature Sensor</b> does not work out of reset. The temperature sensor in the ADC does not work out of reset.	Temperature measurements done using the temperature sensor in the ADC will be wrong without the fix described below.	To enable the temperature sensor, set *0x400C6018 = 0x6. This fix can not be used at the same time as the fix for <i>CMU4</i>	Yes
ADC10	<b>ADC VDD Reference Gives Half Resolution</b> When using the internal VDD reference, the ADC resolution is reduced to 11 bits.	Measurements done with the VDD reference will appear to have been divided by 2.	Double each measurement to give the measurements the correct amplitude, sacrificing one bit of resolution.	Yes

ID	Title/Problem	Effect	Fix/Workaround	Resolved in rev C?
ADC11	<b>ADC References Doubled</b>  In single-ended mode, external and differential references are doubled internally.	The reference doubling results in a decrease of the ADC resolution by one bit. As an example, when using an external reference of 1 V in single ended mode, a signal with values from 0 V to 1 V will result in adc codes from 0 to 2047 instead of the full 0 to 4095.	A temporary fix for the external references is to halve the reference voltage. This will give full resolution, but will not be compatible with devices of later revisions.	Yes
CMU4	<b>Energy Mode Transitions Cause HFRCO Overshoot</b>  In rare situations, transitions between energy modes may cause an overshoot in the HFRCO frequency	When switching between energy modes, there is a slight chance that HFRCO will temporarily overshoot its configured frequency. This overshoot may be up to 50%, and may take the system out of its allowed operating conditions by having a system clock higher than 32 MHz. Note that when the MSC is configured to use zero waitstates when accessing flash, the maximum core frequency is 16 MHz.	To fix issue, set *0x400C6018 = 0xC201. This gives better HFRCO stability at the cost of an increased current consumption in EM0 and EM1 of 10 uA. This fix is not compatible with the fix for ADC8.	Yes
DAC1	<b>DAC Sample-Hold</b>  When the DAC is in sample/hold mode, the DAC output is not correctly held, but drifts faster than specified.	The DAC output starts drifting in the order of 10 mV/us after two DAC clock cycles.	Put the DAC in continuous mode by setting the CONVMODE field in the DACn_CTRL register to CONTINUOUS. The DAC channels will then drive their outputs continuously with the data in the DACn_CHxDATA registers. This mode will maintain the output voltage and refresh is therefore not needed. As the DAC cores are not turned off between samples in continuous mode, the power consumption is somewhat increased compared to sample/hold mode.	Yes
DAC2	<b>DAC Enabling</b>  DAC conversions done closely after enabling the DAC channel are incorrect.	The DAC output takes about 600 us (under typical conditions) to settle after a DAC channel has been enabled via setting field CH0EN in DACn_CH0CTRL (or CH1EN in DACn_CH1CTRL for channel 1). The effect is most visible for the 1.25V and 2.5V internal references.	After enabling a DAC channel, wait 600 us before programming the channel data (via DACn_CH0DATA, DACn_CH1DATA, or DACn_COMBDATA).	Yes
DAC3	<b>DAC Settling</b>  Settling in continuous mode can take up to 200 us. Ringing effects can also be observed on the DAC output.	When applying steps to the DAC, the output may take up to 200 us to settle, the voltage difference may be up to 10 mV. The ringing can be up to 100 mV peak-to-peak depending on load, the oscillations will last no longer than 1 us	No workaround	Yes
DAC4	<b>DAC Sample-Hold/Sample-Off</b>  When a sample/refresh is done while in the sample-hold and sample-off modes, a dip in the DAC output voltage occurs.	The voltage-dip causes noise	Use the DAC continuous mode	Yes

ID	Title/Problem	Effect	Fix/Workaround	Resolved in rev C?
DAC5	<b>DAC startup</b>  When enabling a DAC channel, there may be a transient on the channel output. This transient may be up to 800 mV and last about 1us on an unloaded DAC.	The DAC output is incorrect a short while after enabling the DAC channel.	To prevent the transient on the DAC output, make sure the DAC output is disabled by clearing OUTMODE in DACn_CTRL when enabling a DAC channel.	Yes
DAC6	<b>DAC Monotonicity</b>  DAC output is not monotonic with the input code for some input codes.	For some input codes, e.g. 1024, 2048, 3072, an increase/decrease of one input code will result in an output change equal to up to 3 input codes.	No workaround	Yes
EMU1	<b>EM Transition Brown Out</b>  In rare situations, transitioning between energy modes may cause a Brown Out (BO)	When switching between energy modes, there is a slight chance that the system will experience a BO. In that case, the system will be reset and the error condition can be detected by reading the RMU_RSTCAUSE register, which will then show that an internal BO was the reason for the reset.	To fix issue, set *0x400C6020 = 0x6000. This prevents the BO, but results in an increase of current consumption in EM0 and EM1 by about 4%.	Yes
I2C2	<b>I<sup>2</sup>C Disabled After EM2/EM3</b>  If the USART0 clock is disabled, the I2C will not work when waking up from EM2/EM3	When waking up from EM2/EM3 with the USART0 clock disabled, the I2C module will be in a disabled state until the USART0 clock has been enabled again.	Make sure the USART0 clock is enabled when using the I2C. Alternatively, enable the USART0 clock for a short while after exiting EM2/EM3.	Yes
LCD2	<b>LCD Voltage Boost Current</b>  When the LCD boost target voltage is close to or lower than VDD, the voltage boost function draws an excessive amount of current	If voltage boost is enabled when the boost target voltage, given by VBLEV in LCD_DISPCTRL is lower than or close to VDD, the current consumption of the LCD driver increases by about 500 uA.	Make sure the voltage boost is not enabled before VDD is below the boost target voltage. This can be done by using the VCMP module to monitor VDD and enable/disable voltage boost when VDD goes below/above a given voltage, or by using the ADC to regularly sample VDD.	Yes
LCD3	<b>LCD BLINKEN</b>  If LCD blink is disabled when the display is in the off-period, all segments remains off until LCD blink is enabled again.	When clearing BLINKEN the LCD controller may go to an off-state	Wait until BLINK in LCD_STATUS is set before clearing BLINKEN.	Yes
LEUART2	<b>LEUART Baudrate</b>  The LEUART baudrate generator should have an integral baudrate	For some baudrate settings, the jitter will be higher than +- 0.5 clock cycles, and the average baudrate value will also not be as expected. For ~9600 b/s @ 32.768 kHz oscillator frequency, CLKDIV=0x268 and CLKDIV=0x270	For 9600 b/s @ 32.768 kHz, use CLKDIV=0x270, which gives a baudrate of ~9534 b/s	Yes

ID	Title/Problem	Effect	Fix/Workaround	Resolved in rev C?
	error no larger than +- 0.5 clock cycles. However, the error may be up to 1 clock cycle.	for instance gives significantly different baudrates. For lower baudrates there should be no problem when using a 32 kHz oscillator.		
LFRCO1	<b>LFRCO Frequency</b>  The frequency of the LFRCO changes with up to 30% between EM0/EM1 and EM2/EM3.	Calibrating the LFRCO for a given frequency in EM0/EM1 will not guarantee the same frequency in EM2/EM3.	Use LFXO if an accurate clock frequency is important.	Yes
LFXO2	<b>LFXO Temperature Sensitivity</b>  LFXO may stop when temperature approaches -40C.	When temperature approaches -40C, the LFXO may stop. The LFXO will re-start when temperature rises.	Place a resistor in parallel with the LFXO crystal. The resistor should be between 20 MOhm and 50 MOhm.	Yes
PCNT1	<b>PCNT0 TOP Register</b>  The reset value of the TOP register of PCNT0 is incorrect.	When counting downwards, the pulse counter underflows to an incorrect value. When counting upwards, no interrupt flag is set when counting beyond the maximum value of 0xFF.	Before enabling PCNT0, write the desired top value to the TOPB register. Then load this value into the TOP register by setting LTOPBM in the CMD register.	No
USART1	<b>U(S)ART Double Buffer</b>  Transmission control through TXDATAx and TXDOUBLEX does not work with data double buffering.	When a frame is loaded into the transmission shift register, transmission control bits are always taken from outer buffer element. If only one frame is in the U(S)ART buffer, the content of the buffer elements is equivalent, and transmission control bits work as specified. If two frames are in the buffer however, the control bits for the frame in the outer buffer are used for transmitting the frame in inner buffer. This is not a problem for frames consisting of more than 9 bits, since these large frames occupy both the inner and outer buffer elements.	If using transmission control bits in registers TXDATAx or TXDOUBLEX make sure there are not more than one frame in the U(S)ART buffer at a time, or that the control bits are equal. When TXBL in U(S)ARTn_CTRL is cleared, the TXBL status and interrupt flags in U(S)ARTn_STATUS and U(S)ARTn_IF respectively tell when the buffer is empty. When using transmission control bits, a single frame can then be loaded into the USART for transmission.	No

## 2 Revision History

### 2.1 Revision 1.00

April 23rd, 2010

Removed ADC\_VCM errata.

Updated the erratas whic are to be fixed ir rev C.

### 2.2 Revision 0.10

April 8th, 2010

Initial preliminary release.

## A Disclaimer and Trademarks

### A.1 Disclaimer

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## B Contact Information

### B.1 Energy Micro Corporate Headquarters

Postal Address	Visitor Address	Technical Support
Energy Micro AS P.O. Box 4633 Nydalen N-0405 Oslo NORWAY	Energy Micro AS Sandakerveien 118 N-0405 Oslo NORWAY	support.energymicro.com Phone: +47 40 10 03 01

**www.energymicro.com**

Phone: +47 23 00 98 00

Fax: + 47 23 00 98 01

### B.2 Global Contacts

Visit **www.energymicro.com** for information on global distributors and representatives or contact **sales@energymicro.com** for additional information.

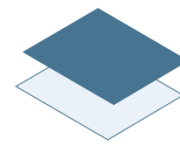
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**ENERGY**<sup>®</sup>  
*micro*

*Energy Micro AS  
Sandakerveien 118  
P.O. Box 4633 Nydalen  
N-0405 Oslo  
Norway*

*[www.energymicro.com](http://www.energymicro.com)*